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of

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10/687,377

**Filing Dat**

October 16, 2003

**First Named Inventor**KO, *et al.*

## Art Unit

TBD

**Examiner Name**

TBD

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
24	A	US-4,631,803	12-30-1986	Hunter, <i>et al.</i>	
	B	US-5,447,884	08-05-1995	Fahey, <i>et al.</i>	
	C	US-5,783,315	08-09-1998	Benedict, <i>et al.</i>	
	D	US-6,020,621	02-01-2000	Wu	
	E	US-6,046,487	04-04-2000	Benedict, <i>et al.</i>	
	F	US-6,251,748 B1	06-26-2001	Hong, <i>et al.</i>	
	G	US-6,285,317 B1	07-24-2001	Chlu, <i>et al.</i>	
	H	US-6,291,321 B1	08-18-2001	Fitzgerald	
	I	US-6,391,729 B1	05-21-2002	Hui	
	J	US-6,417,070 B1	07-09-2002	Ballantine, <i>et al.</i>	
	K	US-6,429,061 B1	08-06-2002	Rim	
	L	US-6,461,936 B1	10-08-2002	von Ehrenwall	
	M	US-6,461,937 B1	10-08-2002	Kim, <i>et al.</i>	
	N	US-6,482,718 B2	11-19-2002	Shiozawa, <i>et al.</i>	
	O	US-6,495,424 B2	12-17-2002	Kunikido	

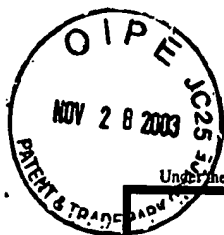
FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	†
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	r <sup>2</sup>
2W	P	SHIMIZU, A., <i>et al.</i> , "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement," International Electron Devices Meeting (2001) pp. 433-436.	
7	Q	THOMPSON, S., <i>et al.</i> , "A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um <sup>2</sup> SRAM Cell," International Electron Devices Meeting (December 2002) pp. 61-64.	
74	R	WELSER, J., <i>et al.</i> , "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," International Electron Devices Meeting (December 1992) pp. 1000-1002.	

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Substitute for form 1449/PTO				<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> (use as many sheets as necessary)				Applicant Number	10/687,377
				Filing Date	October 16, 2003
				First Named Inventor	KO, et al.
				Art Unit	TBD
				Examiner Name	TBD
Sheet	1	of	1	Attorney Docket Number	TSM03-0275

U.S. PATENT DOCUMENTS					
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	C	US-5,783,315	08-09-1998	Benedict, et al.	
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	H	US-6,291,321 B1	09-18-2001	Fitzgerald	
	I	US-6,391,729 B1	05-21-2002	Hui	
	J	US-6,417,070 B1	07-09-2002	Ballantine, et al.	
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	L	US-6,481,936 B1	10-08-2002	von Ehrenwall	
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	<sup>7</sup>
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H	R	WELSER, J., et al., "NMOS and PMOS Transistors Fabricated in Strained Silicon/Relaxed Silicon-Germanium Structures," International Electron Devices Meeting (December 1992) pp. 1000-1002.	

Examiner Signature	<i>R. V. Carrat</i>	Date Considered	10/21/04
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